In the Claims

1. - 32 (canceled)

33. (presently amended) A method of manufacturing a semiconductor device, comprising:

forming a first circuit and a second circuit on a semiconductor wafer substrate assembly;

forming a first conductor connected to the first semiconductor circuit and a second conductor connected to the second semiconductor circuit, wherein the first conductor is electrically separated from the second conductor such that the first and second circuits are sufficiently isolated to provide protection to the second circuit;

with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit with a voltage sufficient to ~~which could~~ damage the second circuit ~~if the first and second circuits were not electrically separate~~ when applied to the first circuit with the first and second circuits electrically connected to each other;

subsequent to performing the electrical operation on the first circuit, shorting the first and second conductors together to electrically couple the first and second circuits; and

subsequent to shorting the first and second conductors together, encapsulating the semiconductor wafer substrate assembly.

34. (previously presented) The method of claim 33 further comprising shorting the first and second conductors together with a ball bond.

35. (presently amended) The method of claim 33 wherein the first and second circuits are fabricated such that the ~~memory~~ semiconductor device is inoperative ~~if~~ when the first and second conductors remain electrically separate subsequent to encapsulation.

36. (previously presented) The method of claim 33 further comprising:

providing a lead frame; and

subsequent to shorting the first and second conductors together, attaching the semiconductor wafer substrate assembly to the lead frame.

37. (presently amended) A method of manufacturing a memory device, comprising:

forming a plurality of primary and redundant memory cell locations;

forming antifuse circuitry which allows selection of the redundant memory cell locations;

forming voltage sensitive circuitry on the semiconductor wafer substrate assembly;

forming a first conductor electrically connected with the antifuse circuitry;

forming a second conductor electrically connected with the voltage sensitive circuitry, wherein the first and second conductors are electrically separated from each other;

while the first and second conductors are electrically separated, applying a ~~sufficient~~ voltage to the antifuse circuitry to program the antifuse circuitry, wherein the ~~sufficient~~ voltage ~~could~~ is sufficient to damage the voltage sensitive circuitry ~~if~~

when applied to the antifuse circuitry when the first and second conductors ~~were~~ are electrically connected; and

subsequent to programming the antifuse circuitry, electrically shorting the first conductor with the second conductor.

38. (previously presented) The method of claim 37 further comprising encapsulating the antifuse circuitry, the voltage sensitive circuitry, the first conductor, and the second conductor subsequent to electrically shorting the first conductor with the second conductor.

39. (previously presented) The method of claim 37 further comprising electrically shorting the first conductor with the second conductor using a ball bond.

40. (previously presented) The method of claim 37 wherein the antifuse circuitry and the voltage sensitive circuitry are fabricated such that the memory device is inoperative if the first and second conductors remain electrically separated.

41. (previously presented) The method of claim 37 further comprising:

providing a lead frame; and

subsequent to bridging the physical opening, attaching the semiconductor wafer substrate assembly to the lead frame.

42. (presently amended) A method of manufacturing a memory device comprising:

fabricating first and second circuits on a semiconductor wafer substrate assembly, wherein the first and second circuits are adapted to be electrically connected through a common conductor;

fabricating the common conductor with a physical opening to provide an open circuit between the first and second circuits, such that the first circuit is sufficiently isolated from the second circuit to provide protection for the first circuit from a

voltage applied to the second circuit which is sufficient to damage the first circuit when applied to the second circuit with the physical opening bridged;

applying the voltage to the second circuit; and

subsequent to applying the voltage to the second circuit, bridging the physical opening of the common conductor to electrically connect the first and second circuits together.

43. (previously presented) The method of claim 42 further comprising encapsulating the first and second circuits and the common conductor subsequent to bridging the physical opening.

44. (presently amended) The method of claim ~~420~~ 42 further comprising bridging the physical opening with a ball bond.

45. (previously presented) The method of claim 42 wherein the first and second circuits are fabricated such that the memory device is inoperative if the physical opening remains unbridged.

46. (previously presented) The method of claim 42 further comprising:

providing a lead frame; and

subsequent to bridging the physical opening, attaching the semiconductor wafer substrate assembly to the lead frame.